IS61NLP25636A/IS61NVP25636A
IS61NLP51218A/IS61NVP51218A

256K x 36 and 512K x 18
9Mb, PIPELINE 'NO WAIT' STATE BUS SRAM

MARCH 2008

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{\text{CKE}}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 165-ball PBGA and 119-ball PBGA packages
- Power supply:
  NVP: V_{DD} 2.5V (± 5%), V_{DDQ} 2.5V (± 5%)
  NLP: V_{DD} 3.3V (± 5%), V_{DDQ} 3.3V/2.5V (± 5%)
- JTAG Boundary Scan for PBGA packages
- Industrial temperature available
- Lead-free available

DESCRIPTION

The 9 Meg 'NLP/NVP' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 256K words by 36 bits and 512K words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{\text{CKE}}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

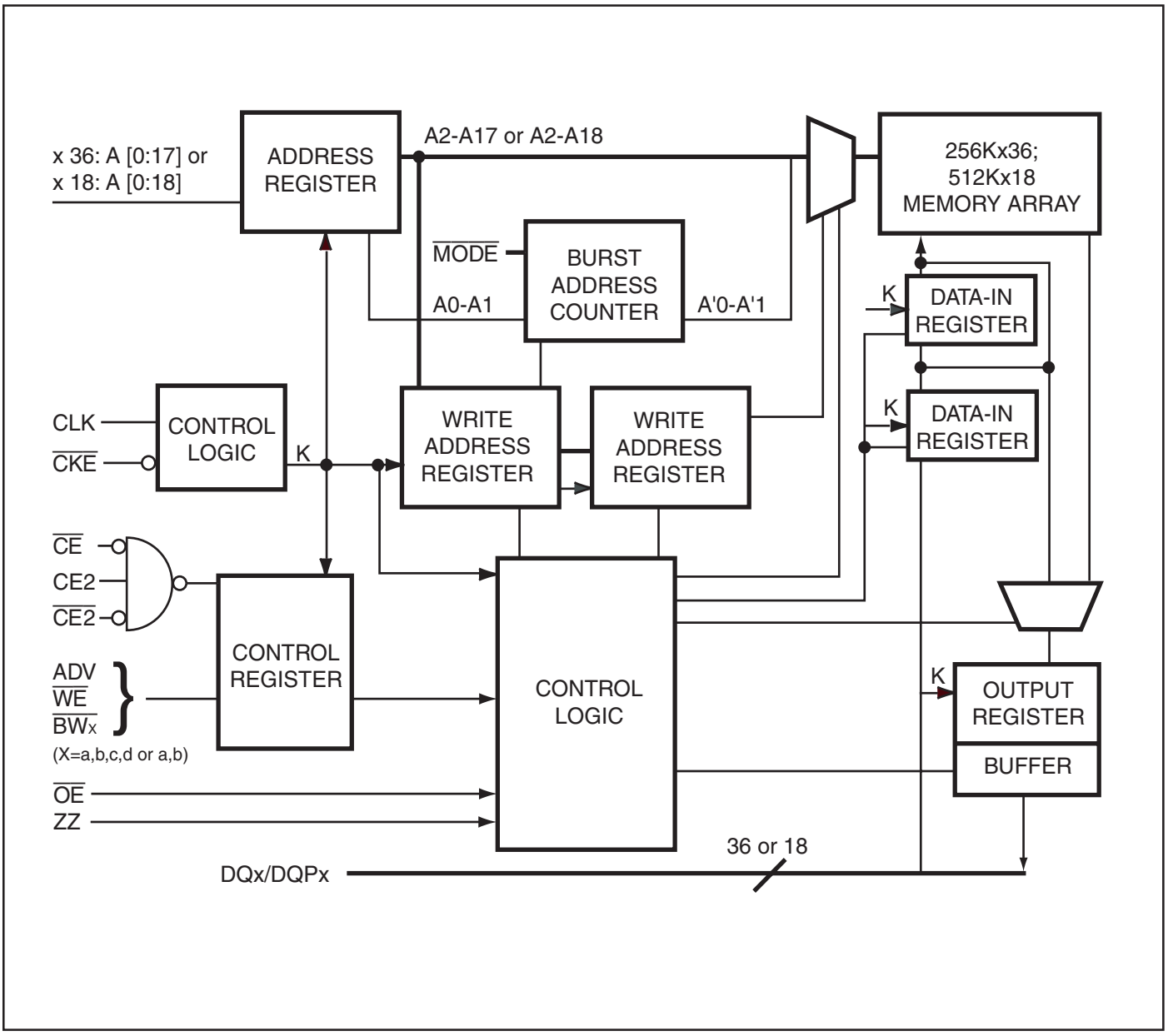
Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{\text{WE}}$ is LOW. Separate byte enables allow individual bytes to be written.

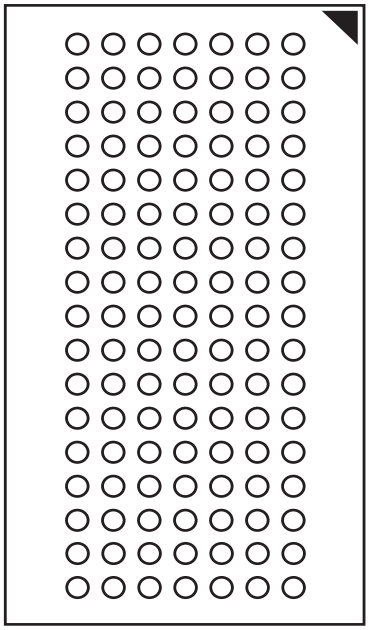
A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

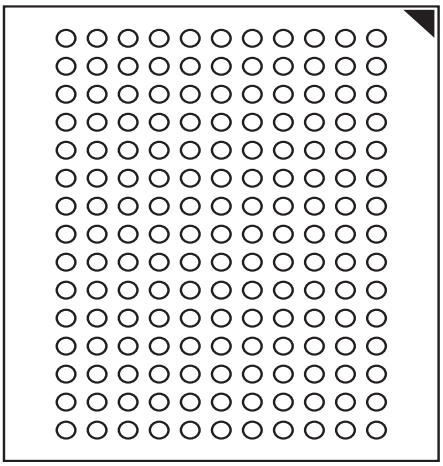
Symbol	Parameter	-250	-200	Units
t_{KQ}	Clock Access Time	2.6	3.1	ns
t_{KC}	Cycle Time	4	5	ns
	Frequency	250	200	MHz

BLOCK DIAGRAM





Bottom View
119-Ball, 14 mm x 22 mm BGA
1 mm Ball Pitch, 7 x 17 Ball Array



Bottom View
165-Ball, 13 mm x 15mm BGA
1 mm Ball Pitch, 11 x 15 Ball Array

PIN CONFIGURATION — 256K x 36, 165-Ball PBGA (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BW}$c	$\overline{BW}$b	$\overline{CE}$2	$\overline{CKE}$	ADV	A	A	NC
B	NC	A	CE2	$\overline{BW}$d	$\overline{BW}$a	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/ Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BW}$x (x=a-d)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode

MODE	Burst Sequence Selection
TCK, TDI TDO, TMS	JTAG Pins
V_{DD}	3.3V/2.5V Power Supply
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
V_{DDQ}	Isolated output Power Supply 3.3V/2.5V
V_{SS}	Ground

119-PIN PBGA PACKAGE CONFIGURATION — 256K x 36 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	$\overline{CE}2$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	Vss	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE}$	Vss	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	Vss	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BW}$c	A	$\overline{BW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{WE}$	Vss	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	Vss	DQa	DQa
L	DQd	DQd	$\overline{BW}$d	NC	$\overline{BW}$a	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CKE}$	Vss	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A_1*	Vss	DQa	DQa
P	DQd	DQPd	V_{SS}	A_0*	Vss	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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ADV	Synchronous Burst Address Advance/ Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$	Synchronous Chip Select
$\overline{CE}2$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{BW}$x (x=a-d)	Synchronous Byte Write Inputs

$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connect
DQa-DQd	Data Inputs/Outputs
DQPa-Pd	Parity Data I/O
V_{DDQ}	Output Power Supply

165-PIN PBGA PACKAGE CONFIGURATION — 512K x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWb}$	NC	$\overline{CE2}$	$\overline{CKE}$	ADV	A	A	A
B	NC	A	CE2	NC	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	NC	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	Vss	NC	NC	NC	Vss	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	$A1^*$	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	$A0^*$	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

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A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
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$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BW}$x (x=a,b)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDI TDO, TMS	JTAG Pins
V_{DD}	3.3V/2.5V Power Supply
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
V_{DDQ}	Isolated output Power Supply 3.3V/2.5V
Vss	Ground

119-PIN PBGA PACKAGE CONFIGURATION — 512K x 18 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	$\overline{CE}2$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	Vss	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CE}$	Vss	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	Vss	DQa	V_{DDQ}
G	NC	DQb	$\overline{BW}$b	A	NC	NC	DQa
H	DQb	NC	V_{SS}	$\overline{WE}$	Vss	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	Vss	NC	DQa
L	DQb	NC	NC	NC	$\overline{BW}$a	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{CKE}$	Vss	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A_1*	Vss	DQa	NC
P	NC	DQPb	V_{SS}	A_0*	Vss	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/ Load
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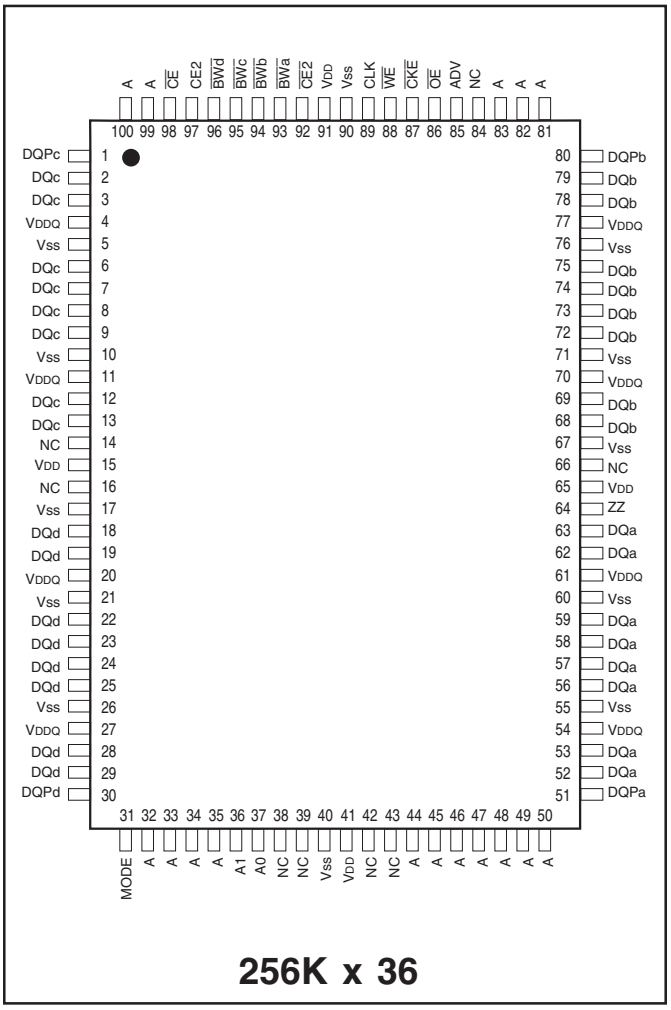
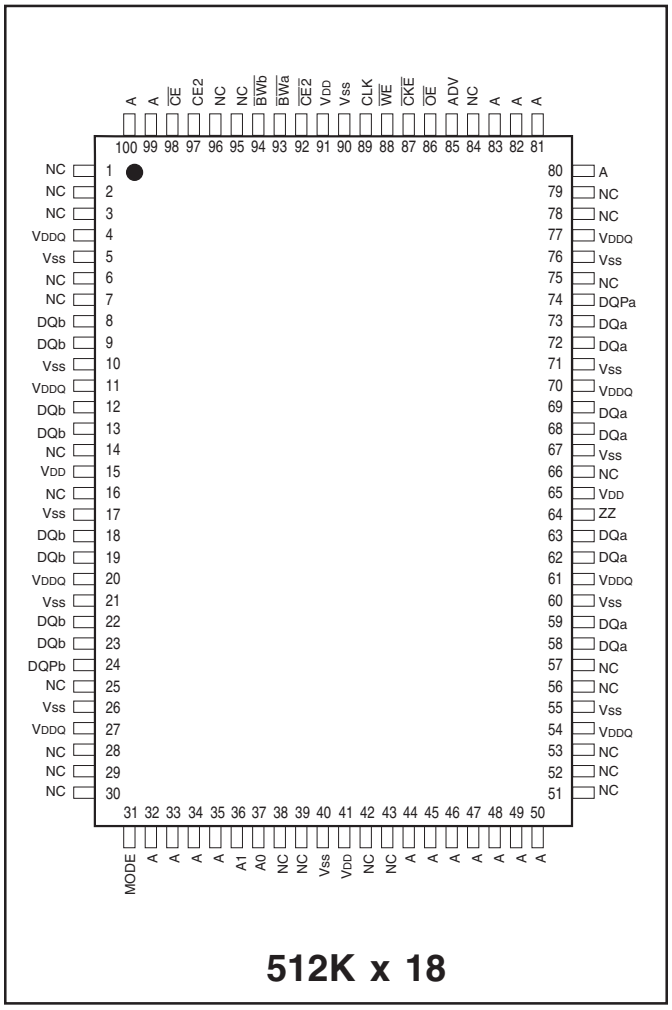
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$	Synchronous Chip Select
$\overline{CE}2$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{BW}$x (x=a,b)	Synchronous Byte Write Inputs

$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connect
DQa-DQb	Data Inputs/Outputs
DQPa-Pb	Parity Data I/O
V_{DDQ}	Output Power Supply

PIN CONFIGURATION
100-Pin TQFP



256K x 36



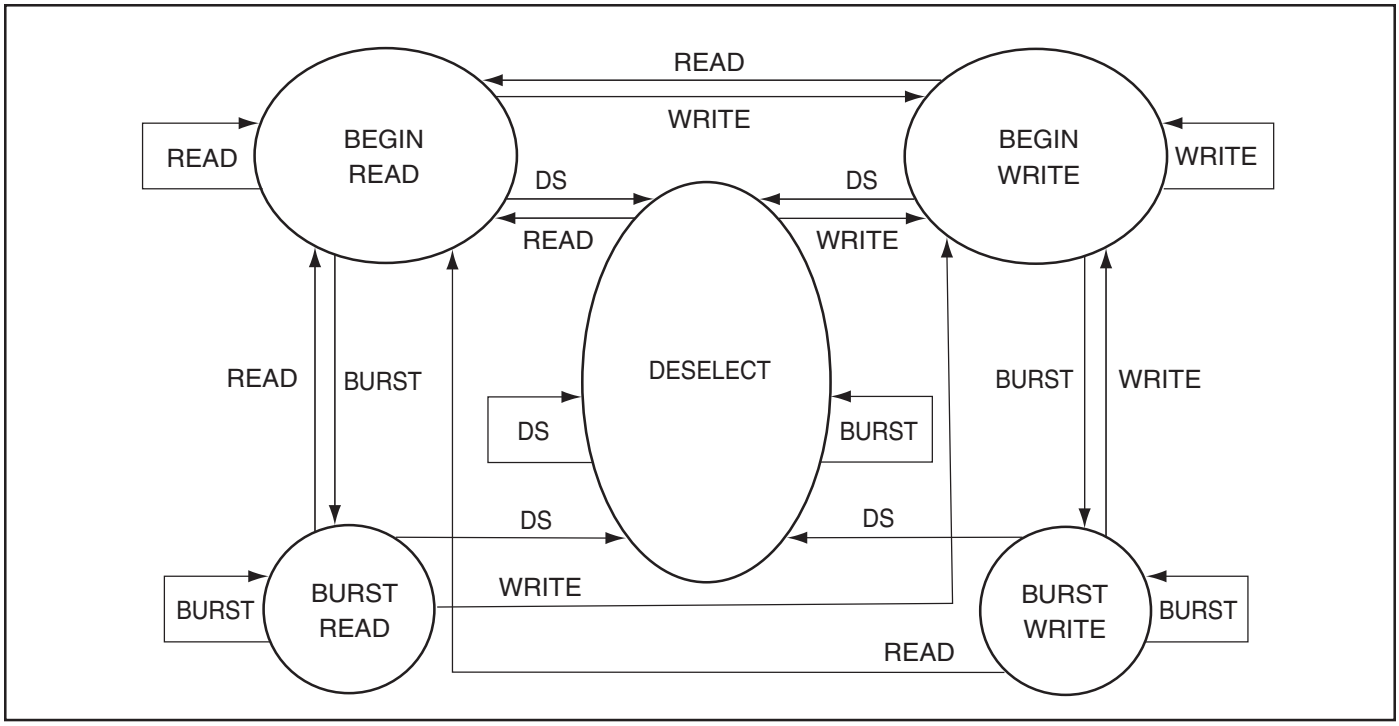
512K x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{BW}$a-$\overline{BW}$d	Synchronous Byte Write Enable
$\overline{WE}$	Write Enable
$\overline{CKE}$	Clock Enable
Vss	Ground for Core
NC	Not Connected

$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data I/O
MODE	Burst Sequence Selection
VDD	+3.3V/2.5V Power Supply
VSS	Ground for output Buffer
VDDQ	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE[1]

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE}2$	ADV	$\overline{WE}$	$\overline{BW}x$	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WE}$ = L means Write operation in Write Truth Table.
   $\overline{WE}$ = H means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous pins (ZZ and $\overline{OE}$).

ASYNCHRONOUS TRUTH TABLE(1)

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTEs	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36)

Operation	$\overline{WE}$	$\overline{BW}a$	$\overline{BW}b$	$\overline{BW}c$	$\overline{BW}d$
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

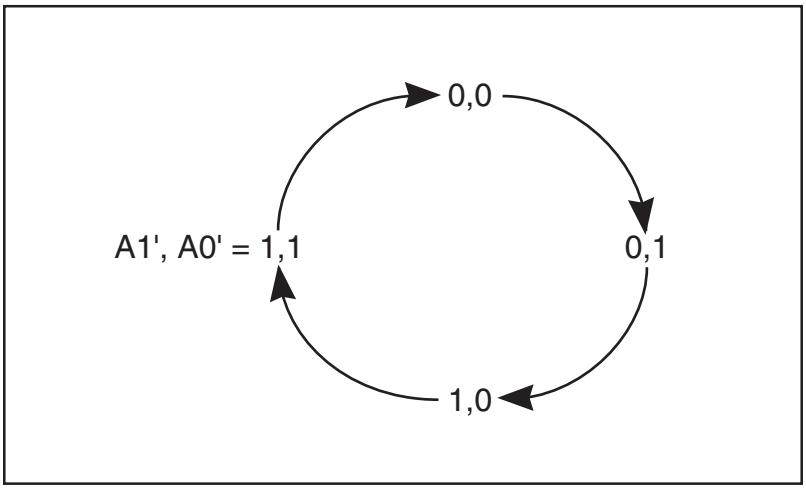
Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to V_{SS} for I/O Pins	–0.5 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to V_{SS} for for Address and Control Inputs	–0.3 to 4.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLPx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61NVPx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	3.3V Min.	3.3V Max.	2.5V Min.	2.5V Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = –1.0 mA (2.5V)	2.4	—	2.0	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.7	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$(1)	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{DDQ}$, $\overline{OE} = V_{IH}$	–5	5	–5	5	µA

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-250 MAX x18	-250 MAX x36	-200 MAX x18	-200 MAX x36	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V, Cycle Time ≥ t_{KC} min.	Com. Ind.	280 300	280 300	270 280	270 280	mA
I_{SB}	Standby Current TTL Input	Device Deselected, V_{DD} = Max., All Inputs ≤ V_{IL} or ≥ V_{IH}, ZZ ≤ V_{IL}, f = Max.	Com. Ind.	100 100	100 100	100 100	100 100	mA
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{DD} = Max., $V_{IN} \le V_{SS}$ + 0.2V or ≥V_{DD} – 0.2V f = 0	Com. Ind.	70 80	70 80	70 80	70 80	mA
I_{SB2}	Sleep Mode	ZZ>V_{IH}	Com. Ind.	45 50	45 50	45 50	45 50	mA

Note:
1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100µA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

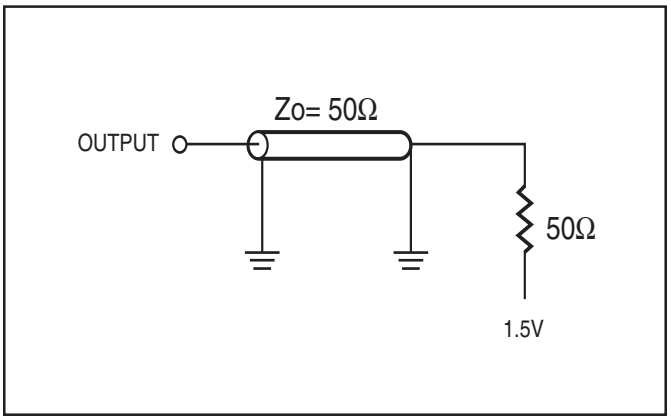


Figure 1

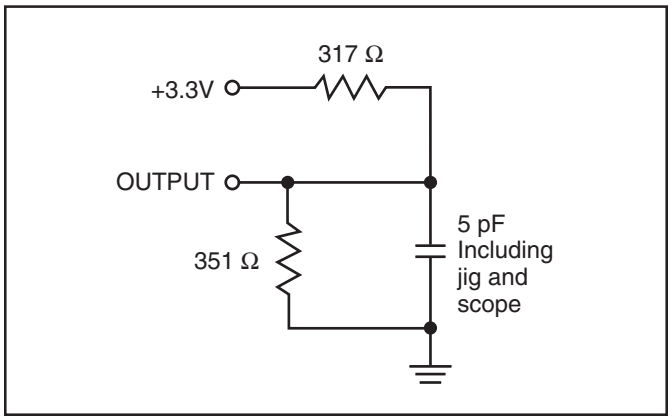


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

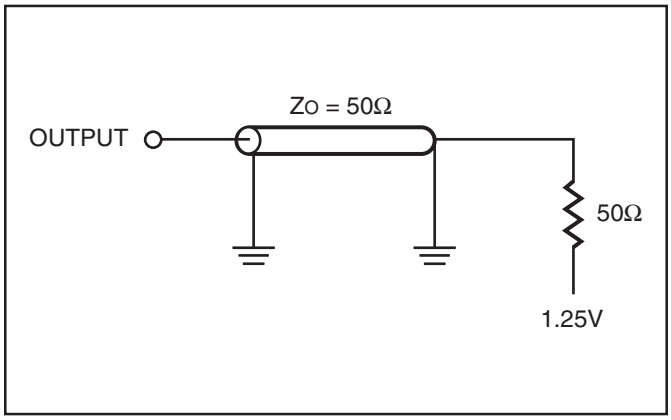


Figure 3

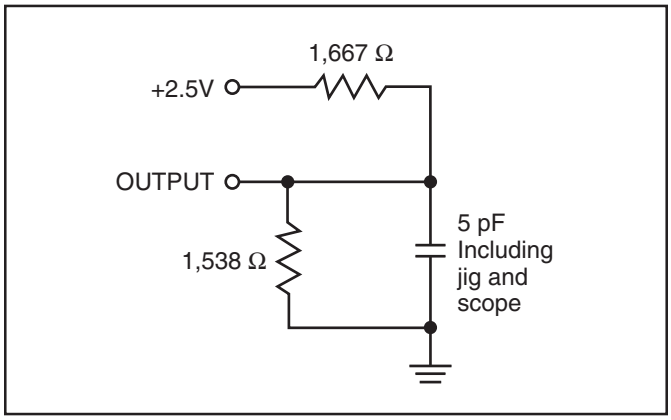


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

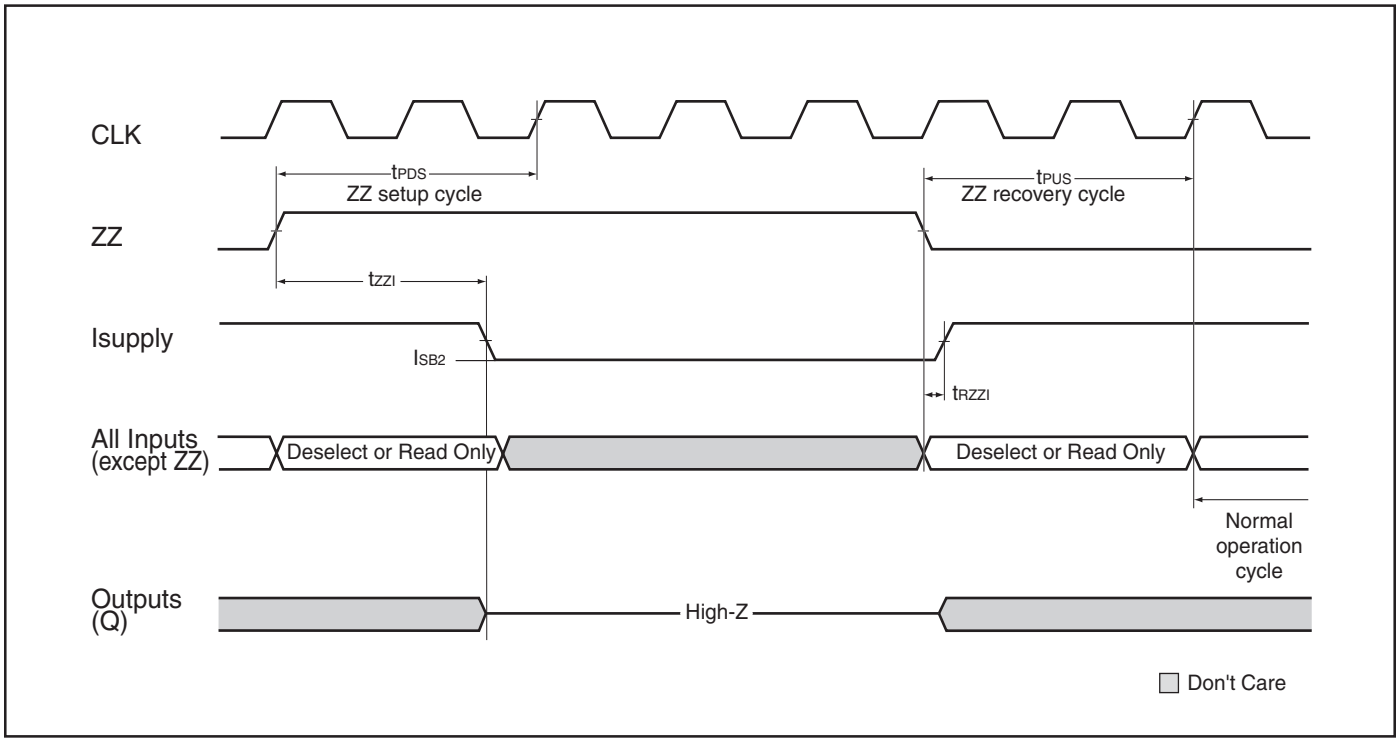
Symbol	Parameter	-250 Min.	-250 Max.	-200 Min.	-200 Max.	Unit
fmax	Clock Frequency	—	250	—	200	MHz
t_{KC}	Cycle Time	4.0	—	5	—	ns
t_{KH}	Clock High Time	1.7	—	2	—	ns
t_{KL}	Clock Low Time	1.7	—	2	—	ns
t_{KQ}	Clock Access Time	—	2.6	—	3.1	ns
t_{KQX}[2]	Clock High to Output Invalid	0.8	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	0.8	—	1	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	2.6	—	3.1	ns
t_{OEQ}	Output Enable to Output Valid	—	2.6	—	3.1	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	2.6	—	3.0	ns
t_{AS}	Address Setup Time	1.2	—	1.4	—	ns
t_{WS}	Read/Write Setup Time	1.2	—	1.4	—	ns
t_{CES}	Chip Enable Setup Time	1.2	—	1.4	—	ns
t_{SE}	Clock Enable Setup Time	1.2	—	1.4	—	ns
t_{ADVS}	Address Advance Setup Time	1.2	—	1.4	—	ns
t_{DS}	Data Setup Time	1.2	—	1.4	—	ns
t_{AH}	Address Hold Time	0.3	—	0.4	—	ns
t_{HE}	Clock Enable Hold Time	0.3	—	0.4	—	ns
t_{WH}	Write Hold Time	0.3	—	0.4	—	ns
t_{CEH}	Chip Enable Hold Time	0.3	—	0.4	—	ns
t_{ADVH}	Address Advance Hold Time	0.3	—	0.4	—	ns
t_{DH}	Data Hold Time	0.3	—	0.4	—	ns
t_{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t_{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

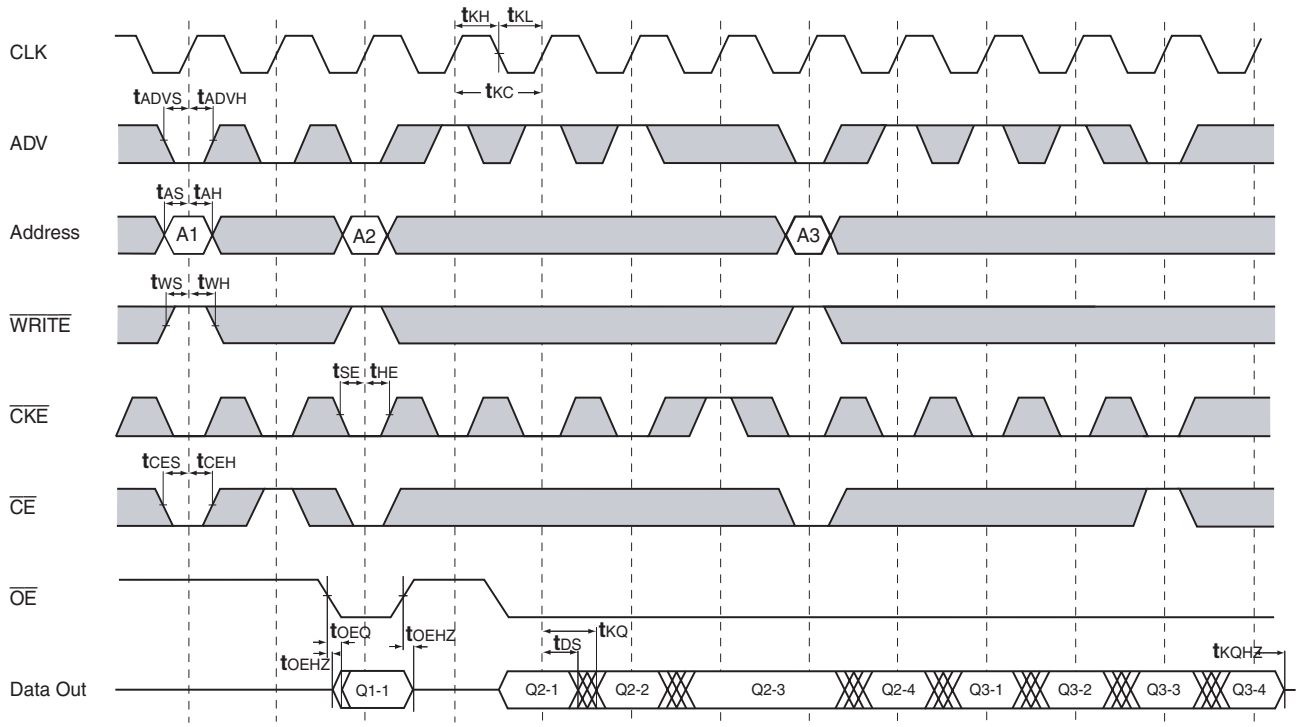
SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SLEEP MODE	ZZ ≥ V_{IH}		60	mA
t_{PDS}	ZZ active to input ignored		2		cycle
t_{PUS}	ZZ inactive to input sampled		2		cycle
t_{ZZI}	ZZ active to SLEEP current		2		cycle
t_{RZZI}	ZZ inactive to exit SLEEP current		0		ns

SLEEP MODE TIMING

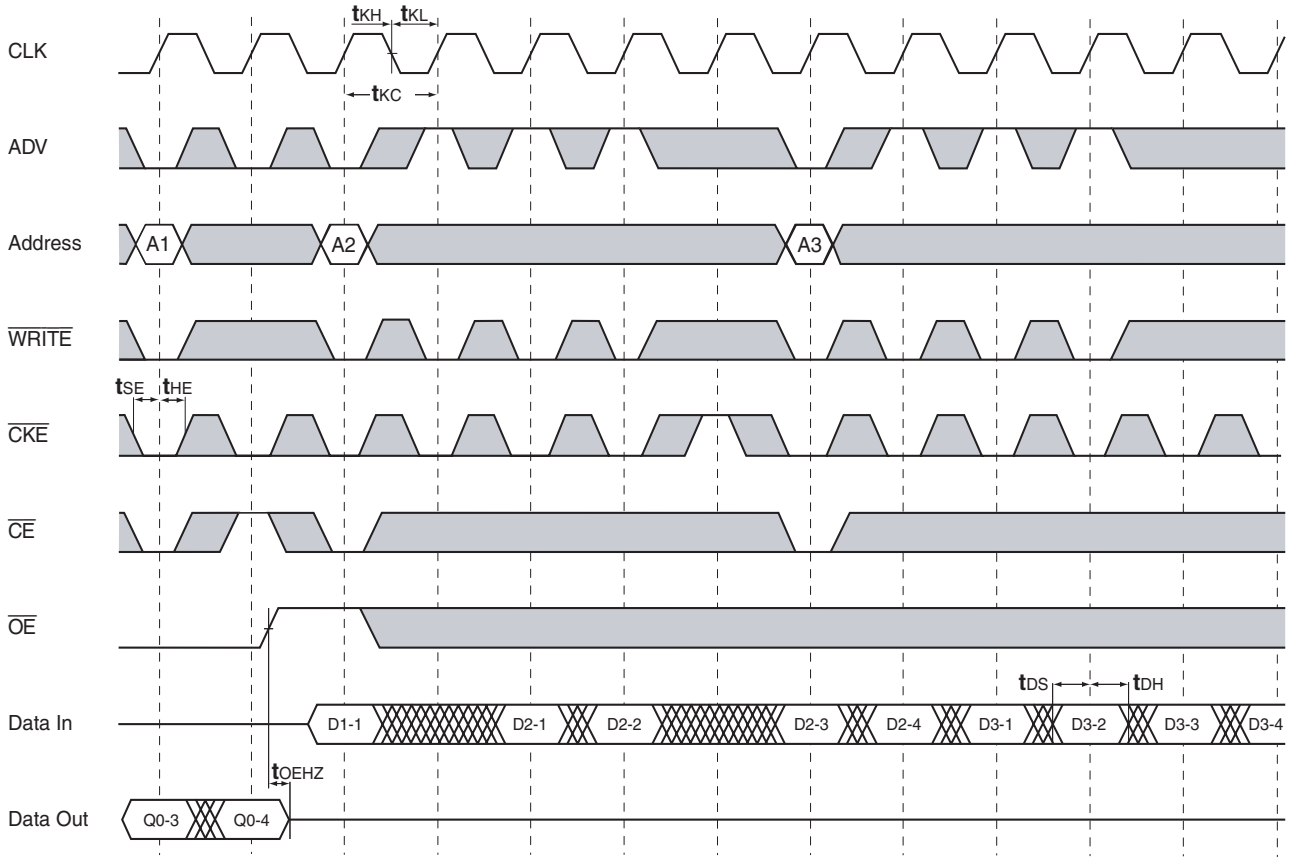


READ CYCLE TIMING

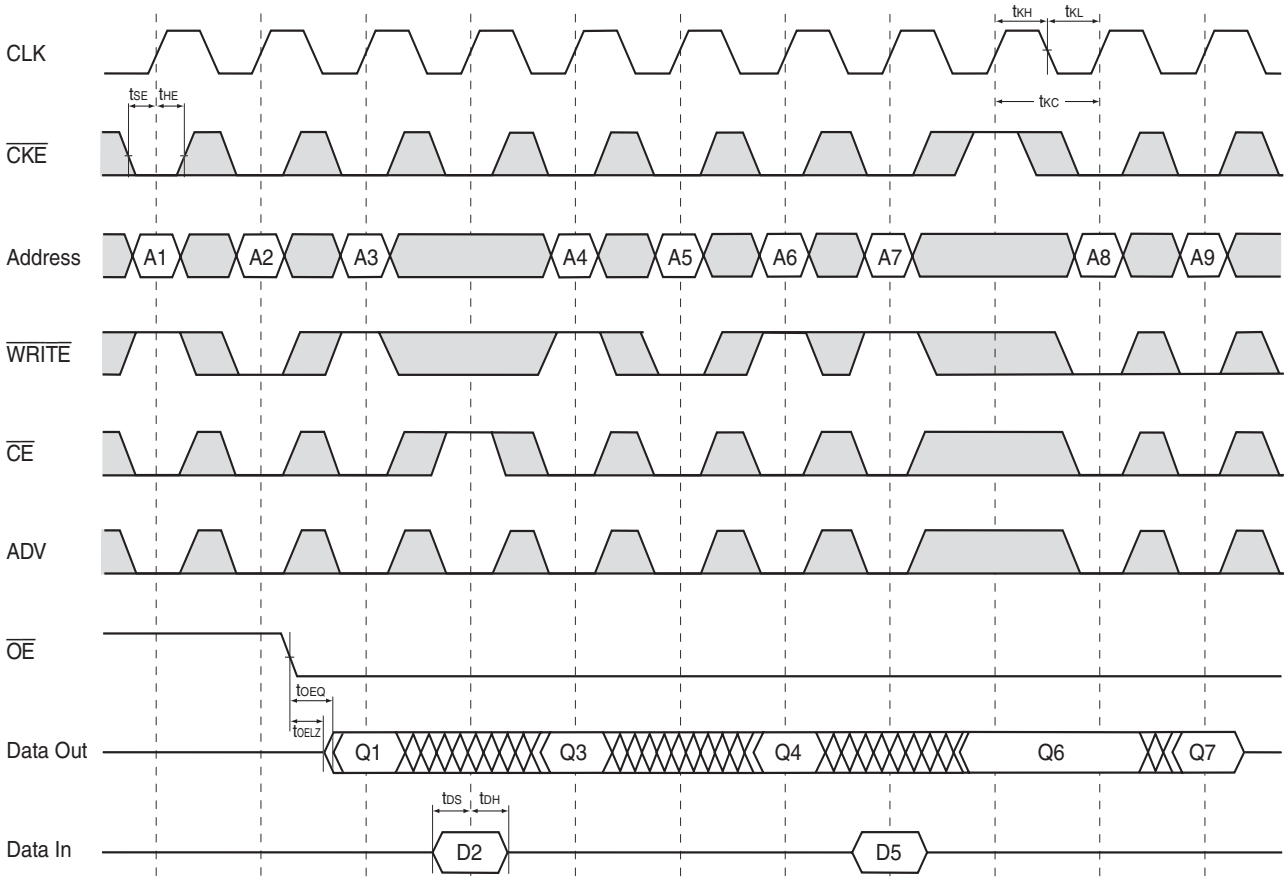


NOTES: $\overline{\text{WRITE}}$ = L means $\overline{\text{WE}}$ = L and $\overline{\text{BW}}$x = L
$\overline{\text{WE}}$ = L and $\overline{\text{BW}}$X = L
$\overline{\text{CE}}$ = L means $\overline{\text{CE}}$1 = L, CE2 = H and $\overline{\text{CE}}$2 = L
$\overline{\text{CE}}$ = H means $\overline{\text{CE}}$1 = H, or $\overline{\text{CE}}$1 = L and $\overline{\text{CE}}$2 = H, or $\overline{\text{CE}}$1 = L and CE2 = L

WRITE CYCLE TIMING



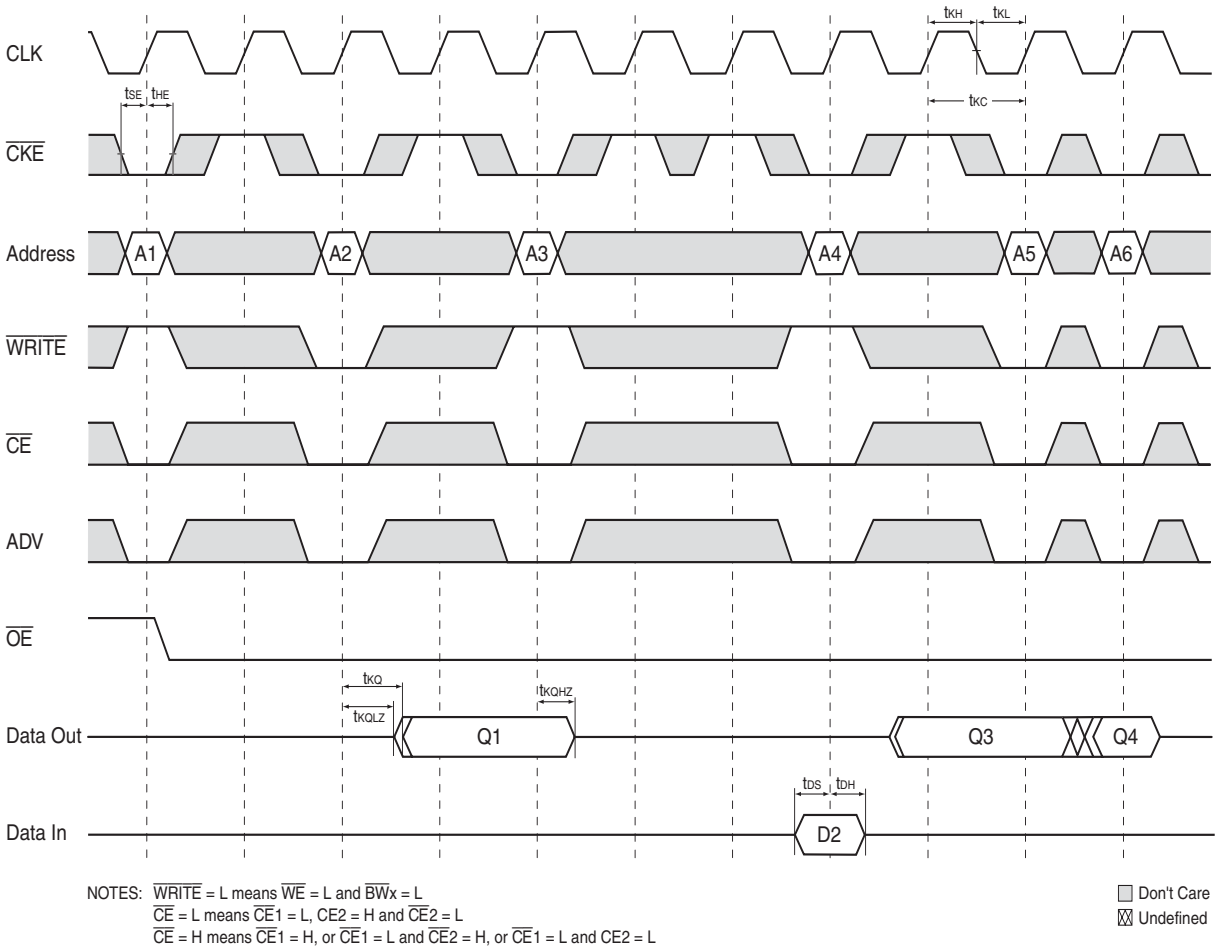
SINGLE READ/WRITE CYCLE TIMING



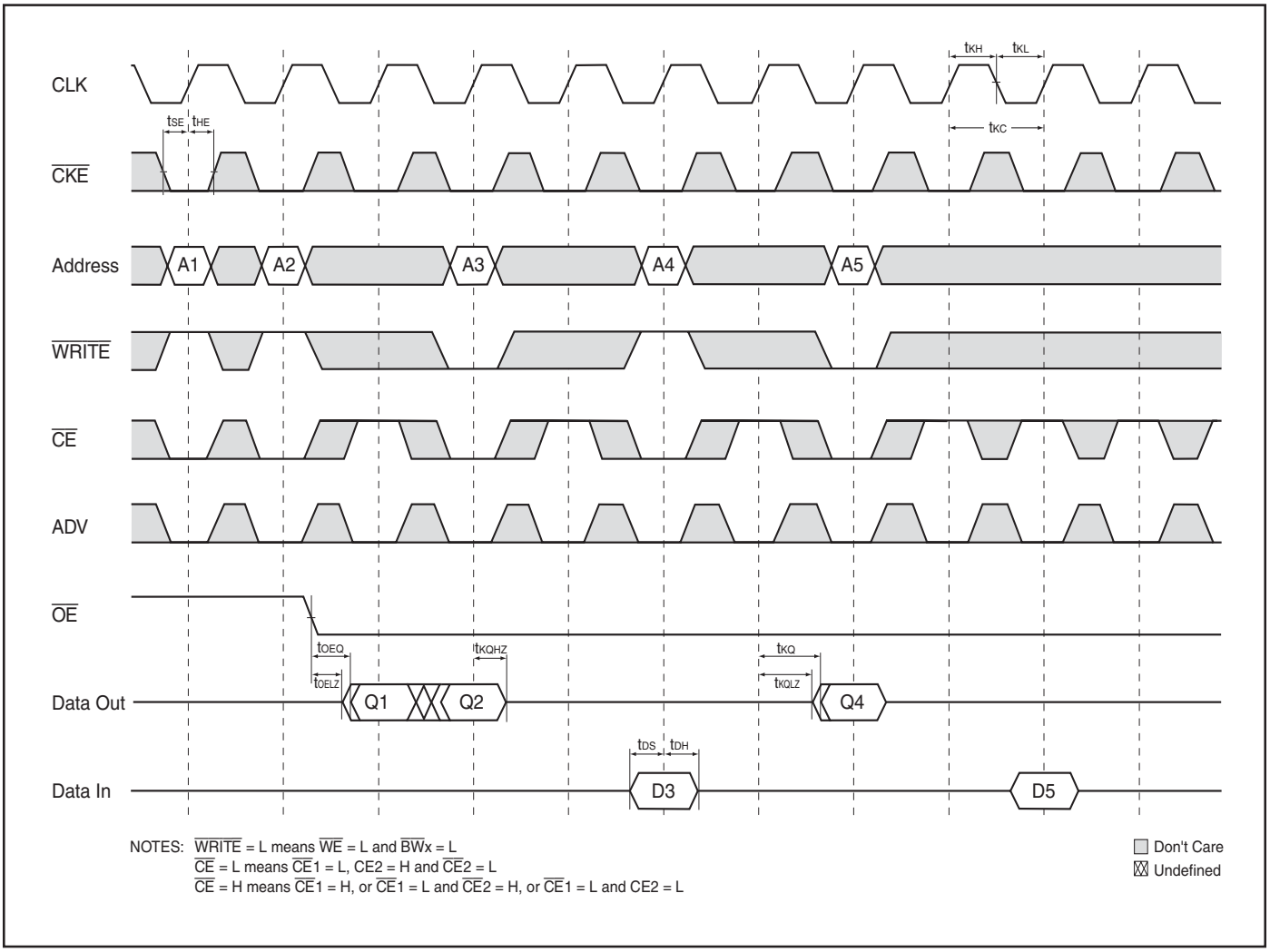
NOTES: WRITE = L means WE = L and BWx = L
CE = L means CE1 = L, CE2 = H and CE2 = L
CE = H means CE1 = H, or CE1 = L and CE2 = H, or CE1 = L and CE2 = L

Don't Care
Undefined

$\overline{CKE}$ OPERATION TIMING



$\overline{CE}$ OPERATION TIMING



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The IS61NLP and IS61NVP have a serial boundary scan Test Access Port (TAP) in the PBGA package only. (Not available in TQFP package.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

DISABLING THE JTAG FEATURE

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

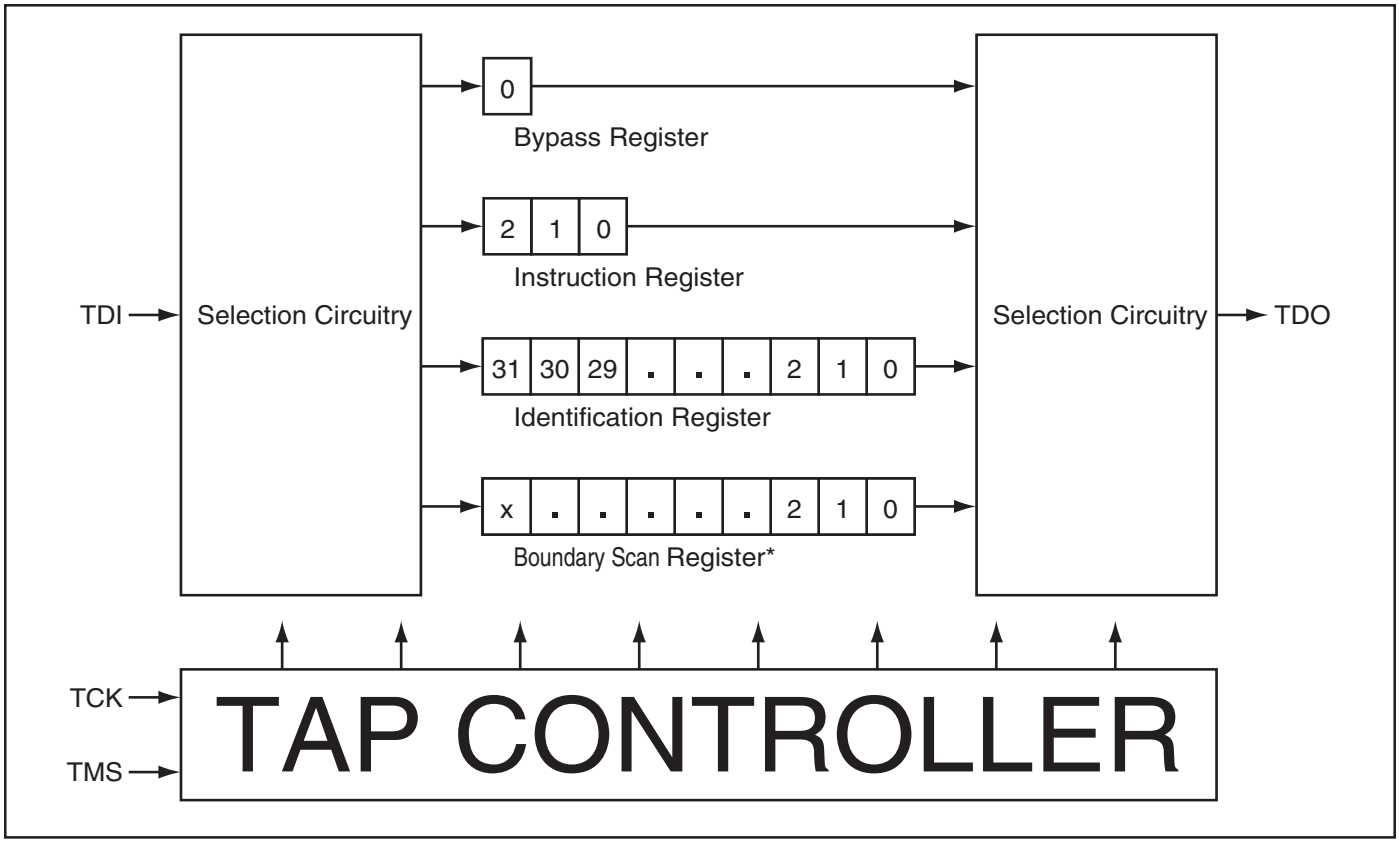
TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

TAP CONTROLLER BLOCK DIAGRAM



TEST DATA OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

PERFORMING A TAP RESET

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 75-bit-long register and the x18 configuration also has a 75-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	75	75

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

IDENTIFICATION REGISTER DEFINITIONS

Instruction Field	Description	256K x 36	512K x 18
Revision Number (31:28)	Reserved for version number.	xxxx	xxxx
Device Depth (27:23)	Defines depth of SRAM. 256K or 512K	00111	01000
Device Width (22:18)	Defines width of the SRAM. x36 or x18	00100	00011
ISSI Device ID (17:12)	Reserved for future use.	xxxxx	xxxxx
ISSI JEDEC ID (11:1)	Allows unique identification of SRAM vendor.	00011010101	00011010101
ID Register Presence (0)	Indicate the presence of an ID register.	1	1

TAP INSTRUCTION SET

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE-Z

The SAMPLE-Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). To insure that the SRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

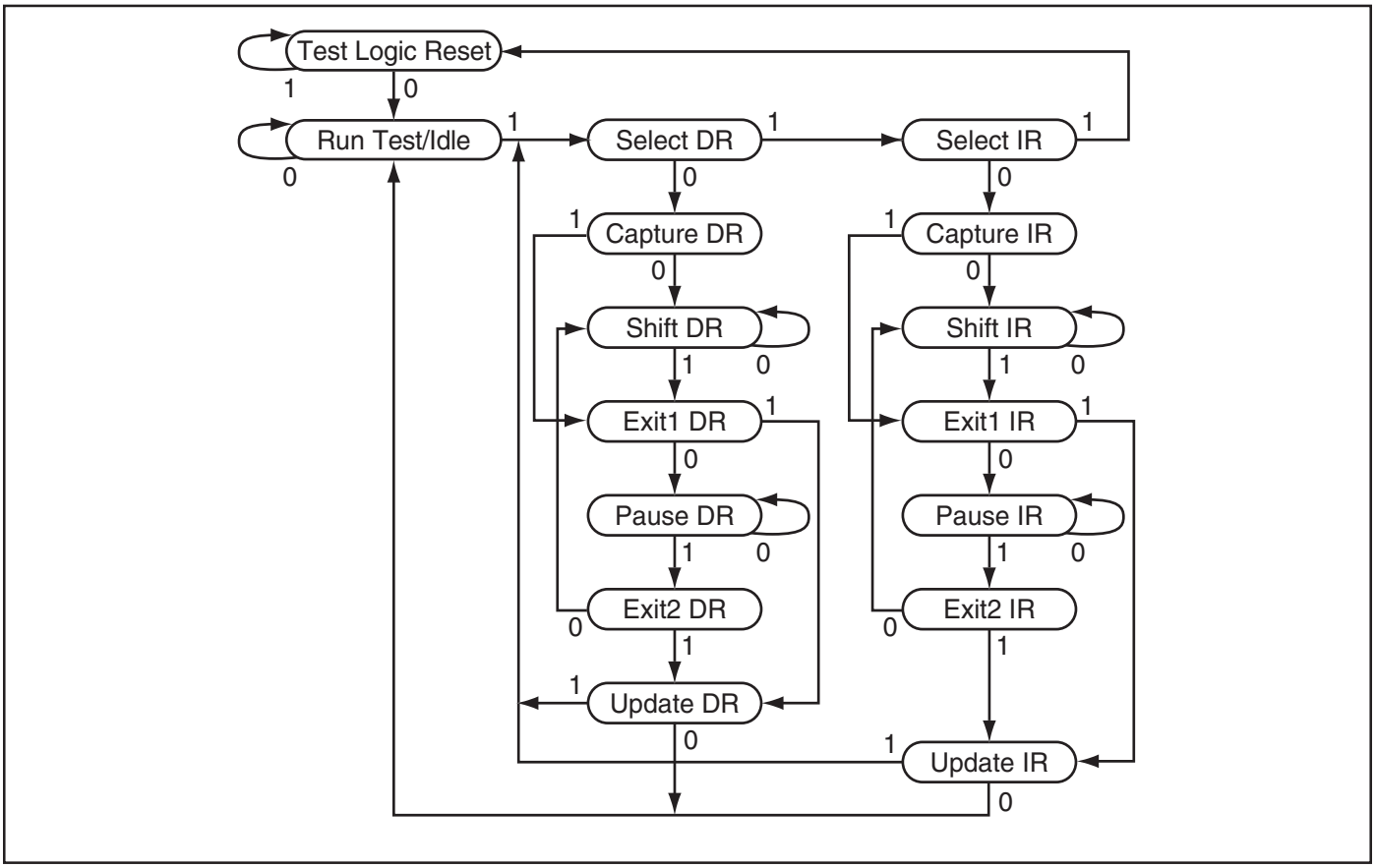
RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

INSTRUCTION CODES

Code	Instruction	Description
000	EXTEST	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
001	IDCODE	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
010	SAMPLE-Z	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
011	RESERVED	Do Not Use: This instruction is reserved for future use.
100	SAMPLE/PRELOAD	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
101	RESERVED	Do Not Use: This instruction is reserved for future use.
110	RESERVED	Do Not Use: This instruction is reserved for future use.
111	BYPASS	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

TAP CONTROLLER STATE DIAGRAM



TAP Electrical Characteristics Over the Operating Range[1,2]

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.7	—	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	2.1	—	V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA	—	0.7	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	—	0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} +0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input Leakage Current	$V_{SS} \le V_I \le V_{DDQ}$	–10	10	µA

Notes:
1. All Voltage referenced to Ground.
2. Overshoot: V_{IH} (AC) $\le$ V_{DD} +1.5V for t $\le$ t_{TCYC}/2,
   Undershoot: V_{IL} (AC) $\le$ 0.5V for t $\le$ t_{TCYC}/2,
   Power-up: V_{IH} < 2.6V and V_{DD} < 2.4V and V_{DDQ} < 1.4V for t < 200 ms.

TAP AC ELECTRICAL CHARACTERISTICS[1,2] (OVER OPERATING RANGE)

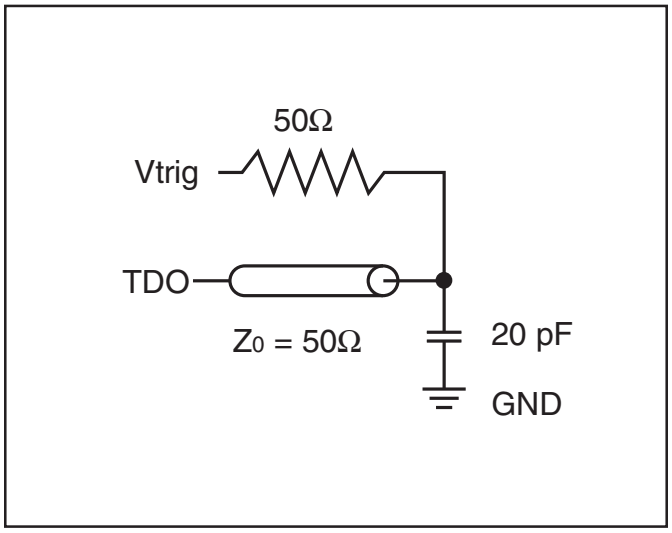
Symbol	Parameter	Min.	Max.	Unit
t_{TCYC}	TCK Clock cycle time	100	—	ns
f_{TF}	TCK Clock frequency	—	10	MHz
t_{TH}	TCK Clock HIGH	40	—	ns
t_{TL}	TCK Clock LOW	40	—	ns
t_{TMSS}	TMS setup to TCK Clock Rise	10	—	ns
t_{TDIS}	TDI setup to TCK Clock Rise	10	—	ns
t_{CS}	Capture setup to TCK Rise	10	—	ns
t_{TMSH}	TMS hold after TCK Clock Rise	10	—	ns
t_{TDIH}	TDI Hold after Clock Rise	10	—	ns
t_{CH}	Capture hold after Clock Rise	10	—	ns
t_{TDOV}	TCK LOW to TDO valid	—	20	ns
t_{TDOX}	TCK LOW to TDO invalid	0	—	ns

Notes:
1. Both t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

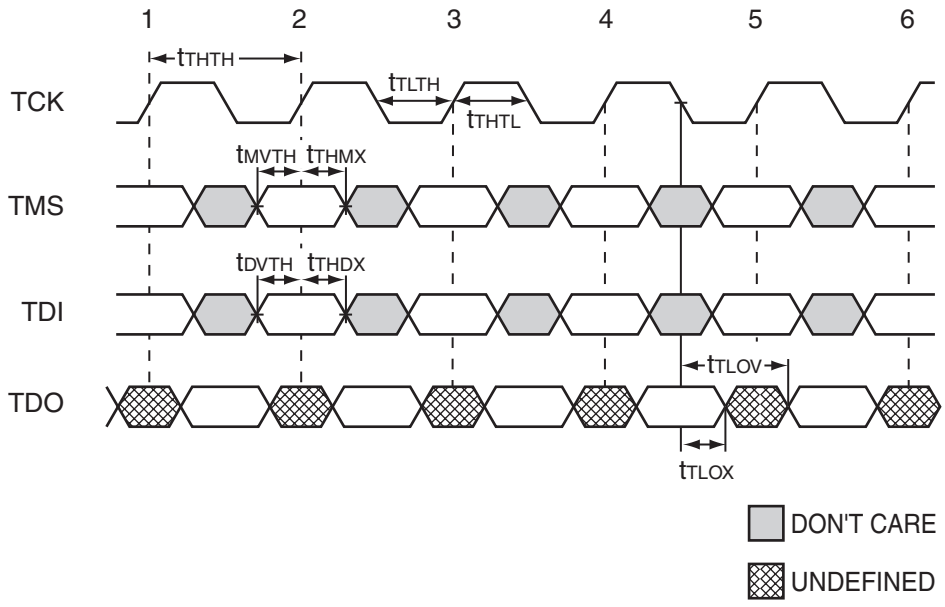
TAP AC TEST CONDITIONS (2.5V/3.3V)

Input pulse levels	0 to 2.5V/0 to 3.0V
Input rise and fall times	1ns
Input timing reference levels	1.25V/1.5V
Output reference levels	1.25V/1.5V
Test load termination supply voltage	1.25V/1.5V
Vtrig	1.25V/1.5V

TAP Output Load Equivalent



TAP TIMING



165 PBGA BOUNDARY SCAN ORDER (x 36)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	MODE	1R	21	DQb	11G	41	NC	1A	61	DQd	1J
2	NC	6N	22	DQb	11F	42	$\overline{CE}$2	6A	62	DQd	1K
3	NC	11P	23	DQb	11E	43	$\overline{BW}$a	5B	63	DQd	1L
4	A	8P	24	DQb	11D	44	$\overline{BW}$b	5A	64	DQd	1M
5	A	8R	25	DQb	10G	45	$\overline{BW}$c	4A	65	DQd	2J
6	A	9R	26	DQb	10F	46	$\overline{BW}$d	4B	66	DQd	2K
7	A	9P	27	DQb	10E	47	CE2	3B	67	DQd	2L
8	A	10P	28	DQb	10D	48	$\overline{CE}$	3A	68	DQd	2M
9	A	10R	29	DQb	11C	49	A	2A	69	DQd	1N
10	A	11R	30	NC	11A	50	A	2B	70	A	3P
11	ZZ	11H	31	A	10A	51	NC	1B	71	A	3R
12	DQa	11N	32	A	10B	52	DQc	1C	72	A	4R
13	DQa	11M	33	A	9A	53	DQc	1D	73	A	4P
14	DQa	11L	34	NC	9B	54	DQc	1E	74	A1	6P
15	DQa	11K	35	ADV	8A	55	DQc	1F	75	A0	6R
16	DQa	11J	36	$\overline{OE}$	8B	56	DQc	1G			
17	DQa	10M	37	$\overline{CKE}$	7A	57	DQc	2D			
18	DQa	10L	38	$\overline{WE}$	7B	58	DQc	2E			
19	DQa	10K	39	CLK	6B	59	DQc	2F			
20	DQa	10J	40	NC	11B	60	DQc	2G			

119 BGA BOUNDARY SCAN ORDER (x 36)

165 PBGA BOUNDARY SCAN ORDER (x 18)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	MODE	1R	21	DQa	11G	41	NC	1A	61	DQb	1J
2	NC	6N	22	DQa	11F	42	$\overline{CE}$2	6A	62	DQb	1K
3	NC	11P	23	DQa	11E	43	$\overline{BW}$a	5B	63	DQb	1L
4	A	8P	24	DQa	11D	44	NC	5A	64	DQb	1M
5	A	8R	25	DQa	11C	45	$\overline{BW}$b	4A	65	DQb	1N
6	A	9R	26	NC	10F	46	NC	4B	66	NC	2K
7	A	9P	27	NC	10E	47	CE2	3B	67	NC	2L
8	A	10P	28	NC	10D	48	$\overline{CE}$	3A	68	NC	2M
9	A	10R	29	NC	10G	49	A	2A	69	NC	2J
10	A	11R	30	A	11A	50	A	2B	70	A	3P
11	ZZ	11H	31	A	10A	51	NC	1B	71	A	3R
12	NC	11N	32	A	10B	52	NC	1C	72	A	4R
13	NC	11M	33	A	9A	53	NC	1D	73	A	4P
14	NC	11L	34	NC	9B	54	NC	1E	74	A1	6P
15	NC	11K	35	ADV	8A	55	NC	1F	75	A0	6R
16	NC	11J	36	$\overline{OE}$	8B	56	NC	1G			
17	DQa	10M	37	$\overline{CKE}$	7A	57	DQb	2D			
18	DQa	10L	38	$\overline{WE}$	7B	58	DQb	2E			
19	DQa	10K	39	CLK	6B	59	DQb	2F			
20	DQa	10J	40	NC	11B	60	DQb	2G			

119 BGA BOUNDARY SCAN ORDER (x 18)

ORDERING INFORMATION (V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V)

Commercial Range: 0°C to +70°C

Access Time	Order Part Number	Package
	256Kx36	
250	IS61NLP25636A-250TQ	100 TQFP
	IS61NLP25636A-250B3	165 PBGA
	IS61NLP25636A-250B2	119 PBGA
200	IS61NLP25636A-200TQ	100 TQFP
	IS61NLP25636A-200B3	165 PBGA
	IS61NLP25636A-200B2	119 PBGA
	512Kx18	
250	IS61NLP51218A-250TQ	100 TQFP
	IS61NLP51218A-250B3	165 PBGA
	IS61NLP51218A-250B2	119 PBGA
200	IS61NLP51218A-200TQ	100 TQFP
	IS61NLP51218A-200B3	165 PBGA
	IS61NLP51218A-200B2	119 PBGA

Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
	256Kx36	
250	IS61NLP25636A-250TQI	100 TQFP
	IS61NLP25636A-250B3I	165 PBGA
	IS61NLP25636A-250B2I	119 PBGA
200	IS61NLP25636A-200TQI	100 TQFP
	IS61NLP25636A-200TQLI	100 TQFP, Lead-free
	IS61NLP25636A-200B3I	165 PBGA
	IS61NLP25636A-200B3LI	165 PBGA, Lead-free
	IS61NLP25636A-200B2I	119 PBGA
	IS61NLP25636A-200B2LI	119 PBGA, Lead-free
	512Kx18	
250	IS61NLP51218A-250TQI	100 TQFP
	IS61NLP51218A-250B3I	165 PBGA
	IS61NLP51218A-250B2I	119 PBGA
200	IS61NLP51218A-200TQI	100 TQFP
	IS61NLP51218A-200TQLI	100 TQFP, Lead-free
	IS61NLP51218A-200B3I	165 PBGA
	IS61NLP51218A-200B2I	119 PBGA

ORDERING INFORMATION (V_{DD} = 2.5V/V_{DDQ} = 2.5V)

Commercial Range: 0°C to +70°C

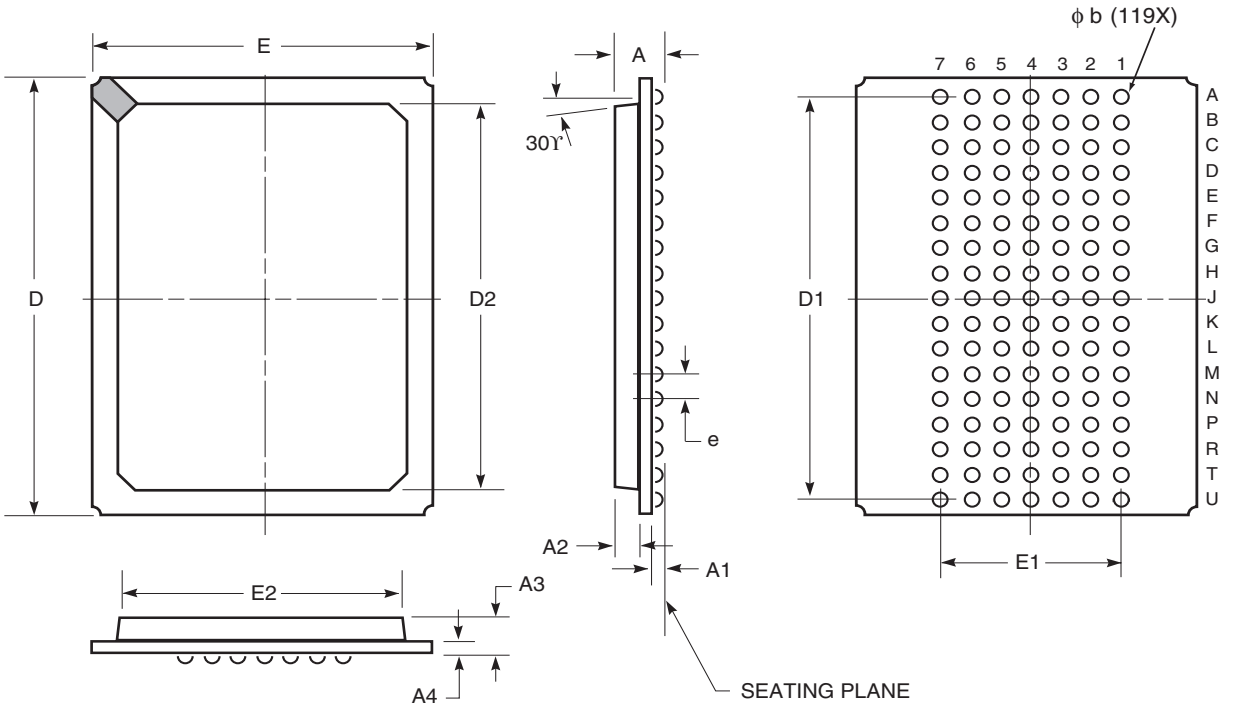
Access Time	Order Part Number	Package
	256Kx36	
250	IS61NVP25636A-250TQ	100 TQFP
	IS61NVP25636A-250B3	165 PBGA
	IS61NVP25636A-250B2	119 PBGA
200	IS61NVP25636A-200TQ	100 TQFP
	IS61NVP25636A-200B3	165 PBGA
	IS61NVP25636A-200B2	119 PBGA
	512Kx18	
250	IS61NVP51218A-250TQ	100 TQFP
	IS61NVP51218A-250B3	165 PBGA
	IS61NVP51218A-250B2	119 PBGA
200	IS61NVP51218A-200TQ	100 TQFP
	IS61NVP51218A-200B3	165 PBGA
	IS61NVP51218A-200B2	119 PBGA

Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
	256Kx36	
250	IS61NVP25636A-250TQI	100 TQFP
	IS61NVP25636A-250B3I	165 PBGA
	IS61NVP25636A-250B2I	119 PBGA
200	IS61NVP25636A-200TQI	100 TQFP
	IS61NVP25636A-200TQLI	100 TQFP, Leadfree
	IS61NVP25636A-200B3I	165 PBGA
	IS61NVP25636A-200B2I	119 PBGA
	512Kx18	
250	IS61NVP51218A-250TQI	100 TQFP
	IS61NVP51218A-250B3I	165 PBGA
	IS61NVP51218A-250B2I	119 PBGA
200	IS61NVP51218A-200TQI	100 TQFP
	IS61NVP51218A-200B3I	165 PBGA
	IS61NVP51218A-200B2I	119 PBGA

PACKAGING INFORMATION

Plastic Ball Grid Array
Package Code: B (119-pin)



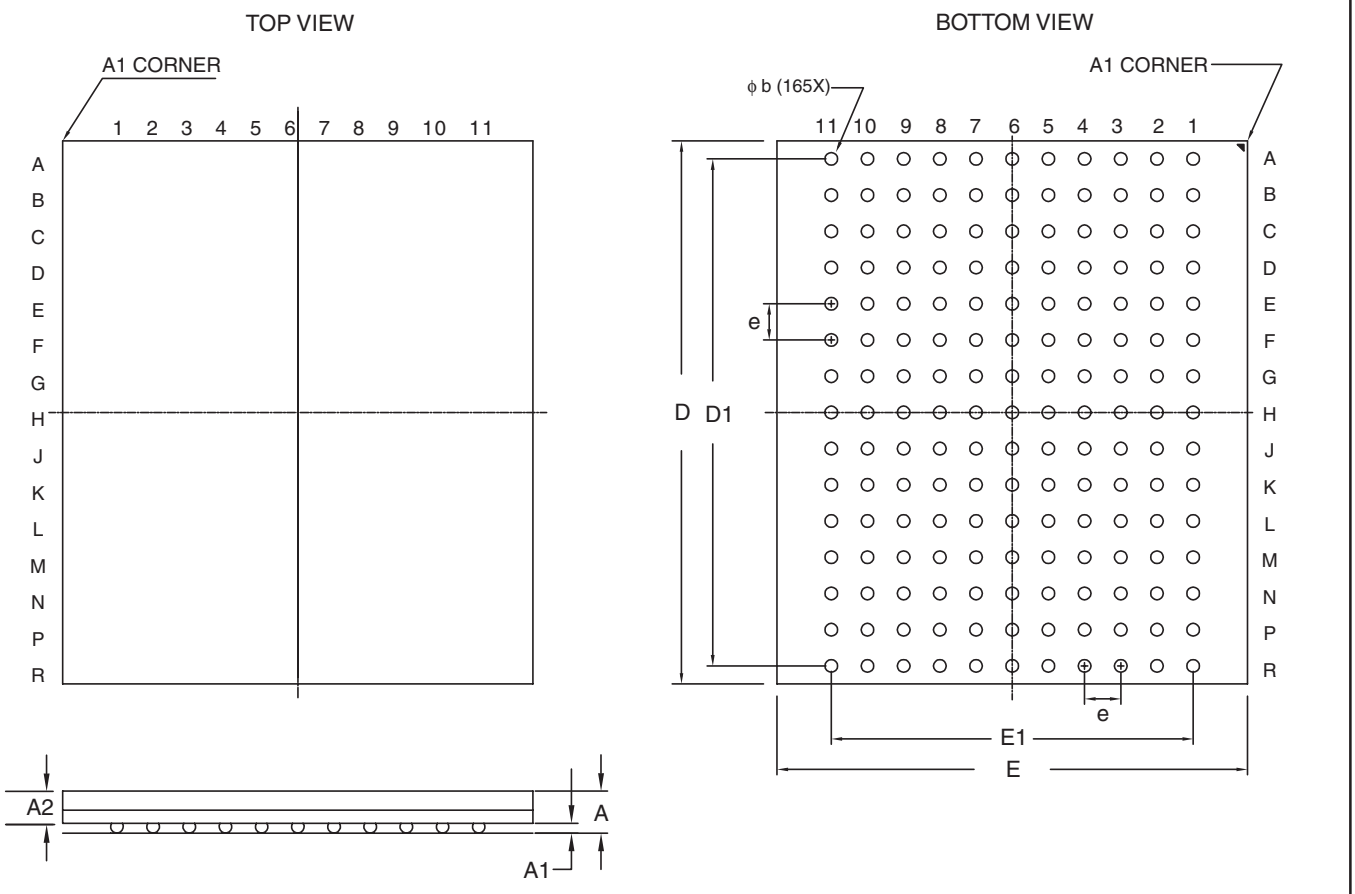
	MILLIMETERS		INCHES	
Sym.	**Min.**	**Max.**	**Min.**	**Max.**
N0. Leads		**119**		
A	—	2.41	—	0.095
A1	0.50	0.70	0.020	0.028
A2	0.80	1.00	0.032	0.039
A3	1.30	1.70	0.051	0.067
A4	0.56 BSC		0.022 BSC	
b	0.60	0.90	0.024	0.035
D	21.80	22.20	0.858	0.874
D1	20.32 BSC		0.800 BSC	
D2	19.40	19.60	0.764	0.772
E	13.80	14.20	0.543	0.559
E1	7.62 BSC		0.300 BSC	
E2	11.90	12.10	0.469	0.476
e	1.27 BSC		0.050 BSC	

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusion and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Ball Grid Array
Package Code: B (165-pin)



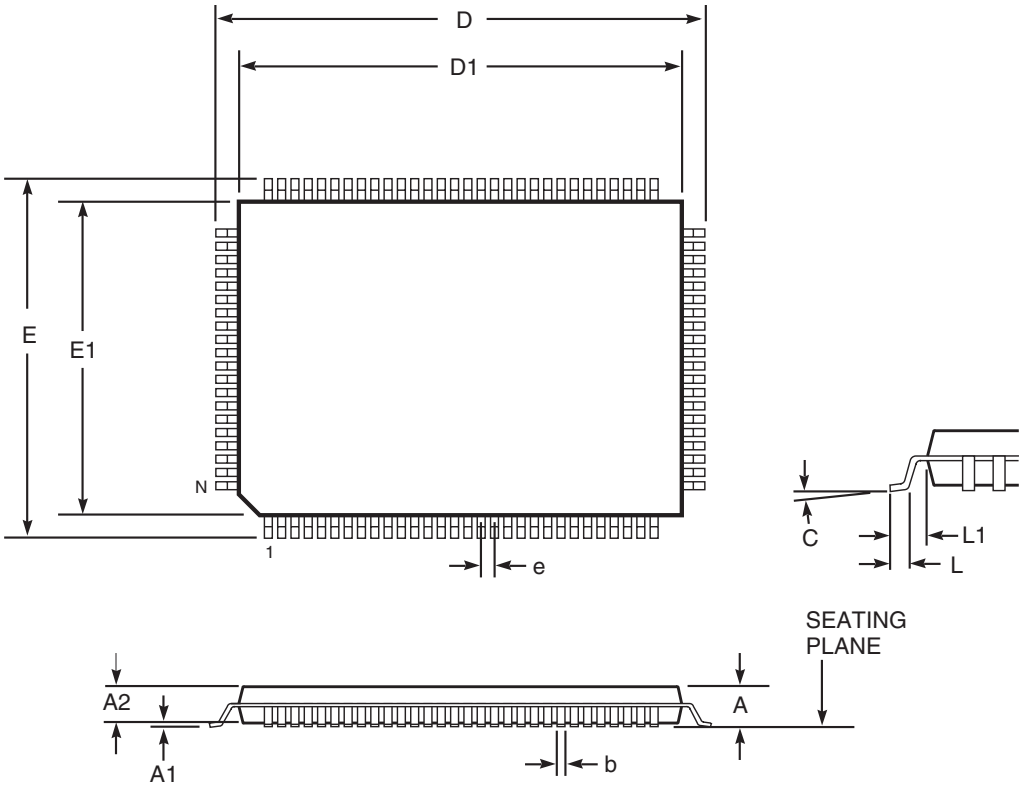
BGA - 13mm x 15mm

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
N0. Leads		**165**			**165**	
A	—	—	1.20	—	—	0.047
A1	0.25	0.33	0.40	0.010	0.013	0.016
A2	—	0.79	—	—	0.031	—
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	—	1.00	—	—	0.039	—
b	0.40	0.45	0.50	0.016	0.018	0.020

Notes:
1. Controlling dimensions are in millimeters.

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)
Package Code: TQ



Thin Quad Flat Pack (TQ)								
	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.								
No. Leads (N)	100				128			
A	—	1.60	—	0.063	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015	0.17	0.27	0.007	0.011
D	21.90	22.10	0.862	0.870	21.80	22.20	0.858	0.874
D1	19.90	20.10	0.783	0.791	19.90	20.10	0.783	0.791
E	15.90	16.10	0.626	0.634	15.80	16.20	0.622	0.638
E1	13.90	14.10	0.547	0.555	13.90	14.10	0.547	0.555
e	0.65 BSC		0.026 BSC		0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030	0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.		1.00 REF.		0.039 REF.	
C	0°	7°	0°	7°	0°	7°	0°	7°

Notes:
1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.